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4	CPU-CLK/Control/MISC/PEG
5	CPU-Memory
6	CPU-Power
7	CPU-GND
8	DDR III DIMM 1 / DIMM 2
9	DDR III DIMM 3 / DIMM 4
10	PCH-PCIE/DMI/USB/CLK
11	PCH-SATA/HOST/GPIO/DDI/VGA
12	PCH-SMB/LPC/AUDIO/RTC
13	PCH-Power
14	PCH-GND
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28	ATX/F_Panel/EMI/LED
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31	VGA
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34	Power Map
35	GPIO Table
36	History

# MS-7829

Version : 0A

## CPU :

**Intel Haswell Processor**

## System Chipset :

**Intel Lynx Point Chipset**

## On Board Chipset :

**VRM 12.5 --ISL95816HRZ 4 Phase**

**Gigabit Intel Clarkville-V I217**

**HDA Codec -- Realtek ALC662-VD**

**Super I/O -- NCT5533D**

**SPI Flash 32Mb**


## Main Memory :

**2 Channel DDR III \* 4 (Max 32GB)**

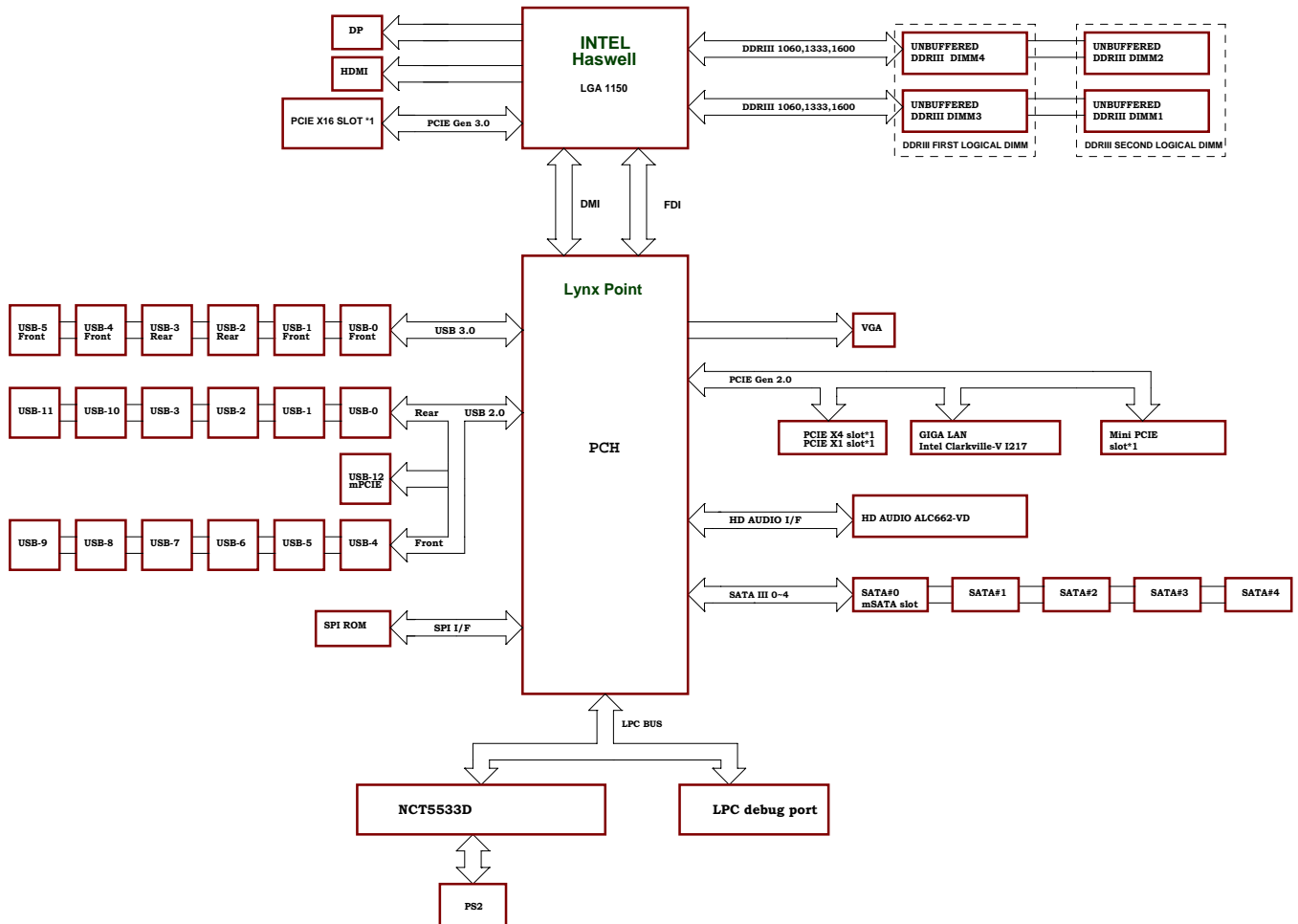
## Expansion Slot :

**PCI Express x16 Slot \* 1**

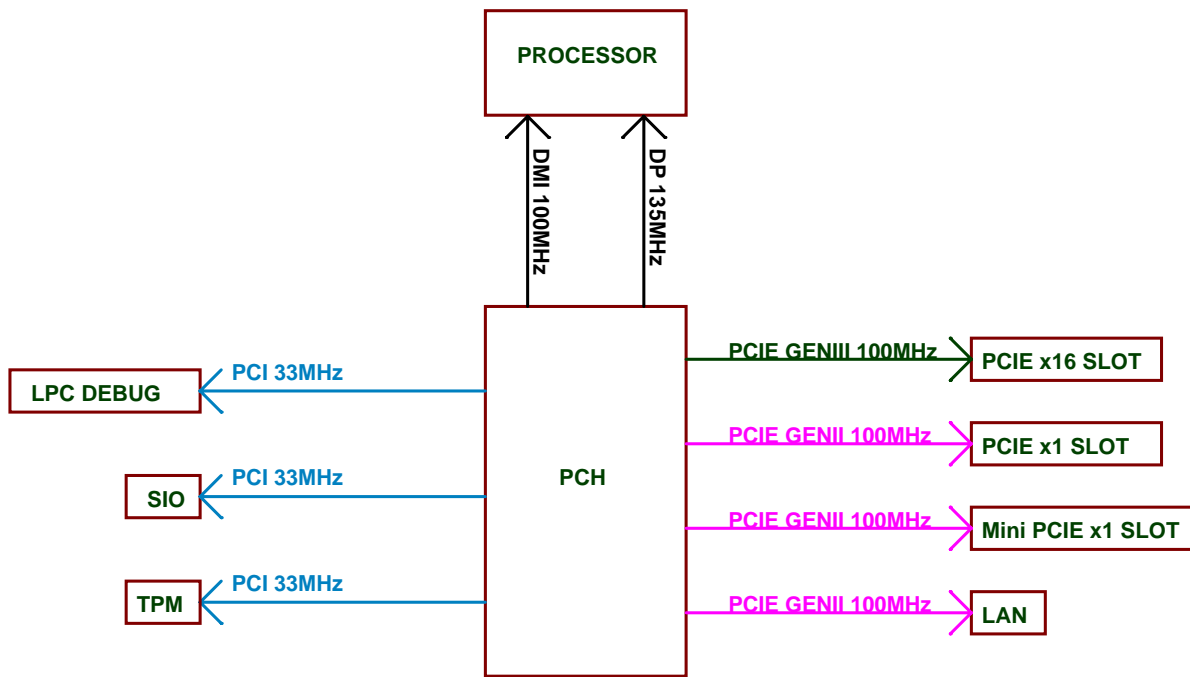
**Mini PCIE/Mini SATA Slot \* 1**

 <b>MICRO-START INTL CO.,LTD.</b>		
File: <b>Cover Sheet</b>		
Size:	Document Number:	Rev:
	<b>Acer SharkBay</b>	<b>0A</b>
Date:	Friday, July 06, 2012	Sheet 1 of 36

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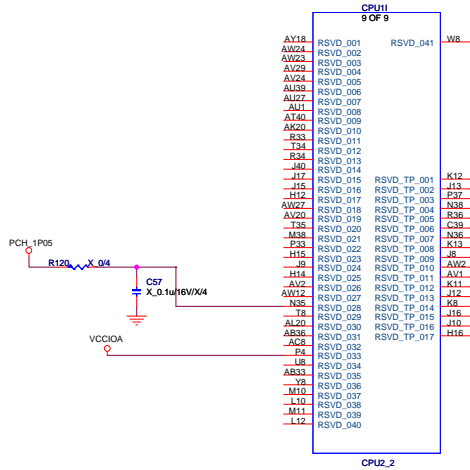
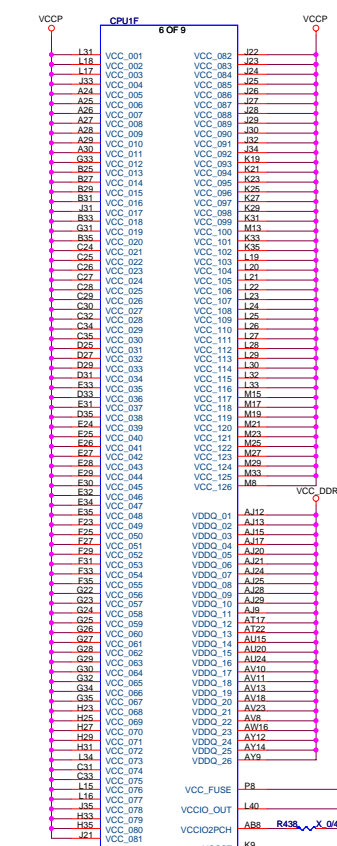
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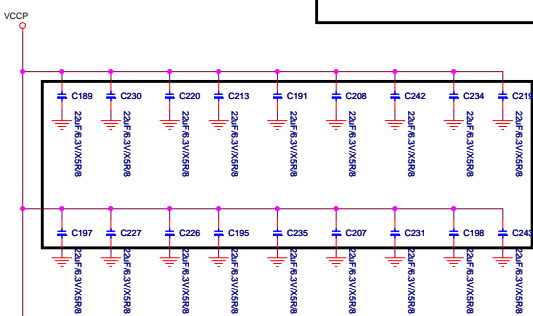




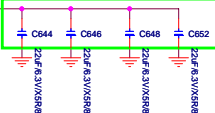


# VCCP-Decoupling

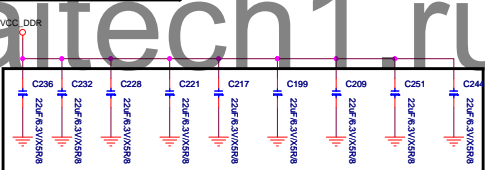
PLACE THESE CAPS INSIDE CPU SOCKET CAVITY



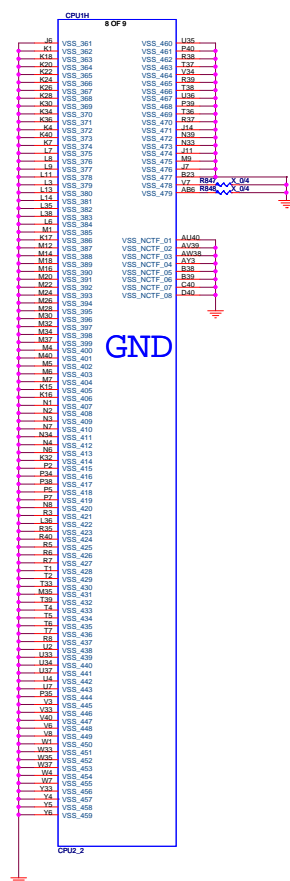
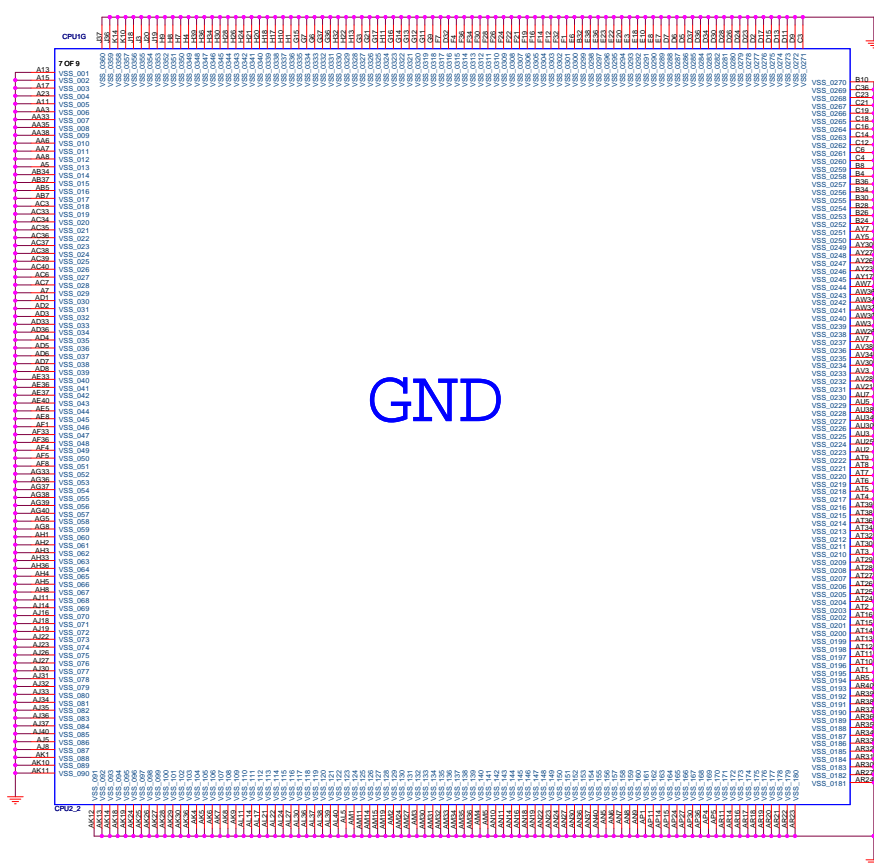
PLACE THESE CAPS NEAR CPU SOCKET EDGE



# VCC\_DDR-Decoupling



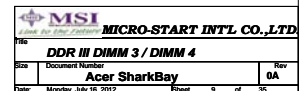
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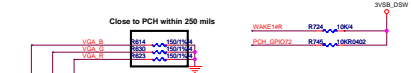
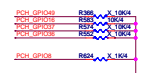
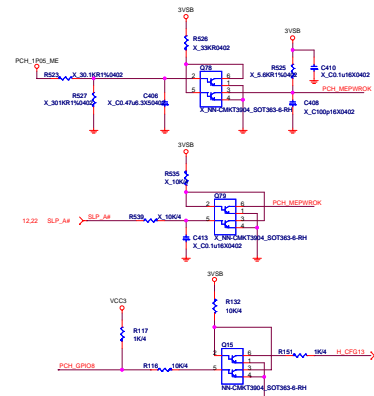
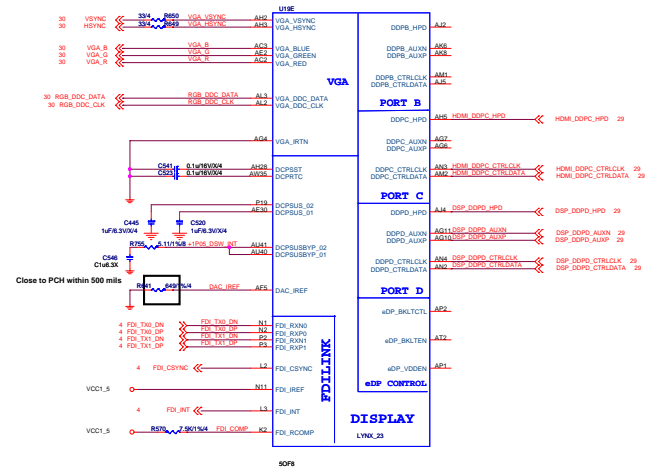
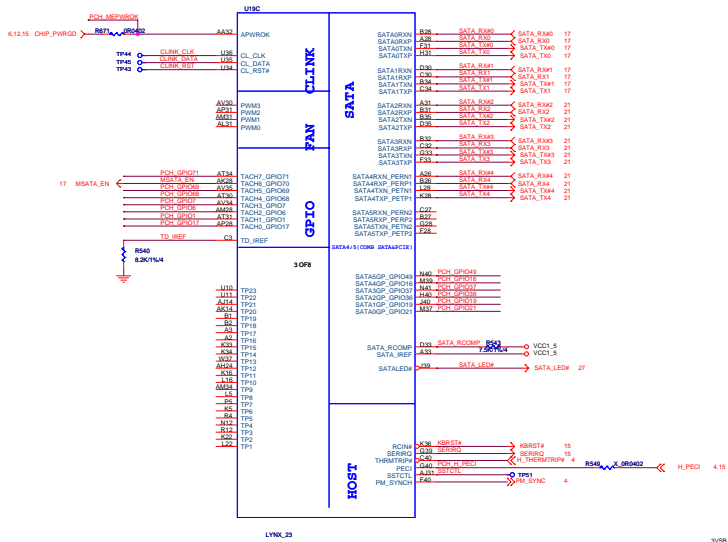
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**DDRIII DIMM\_A2**



**DDRIII DIMM\_B2**





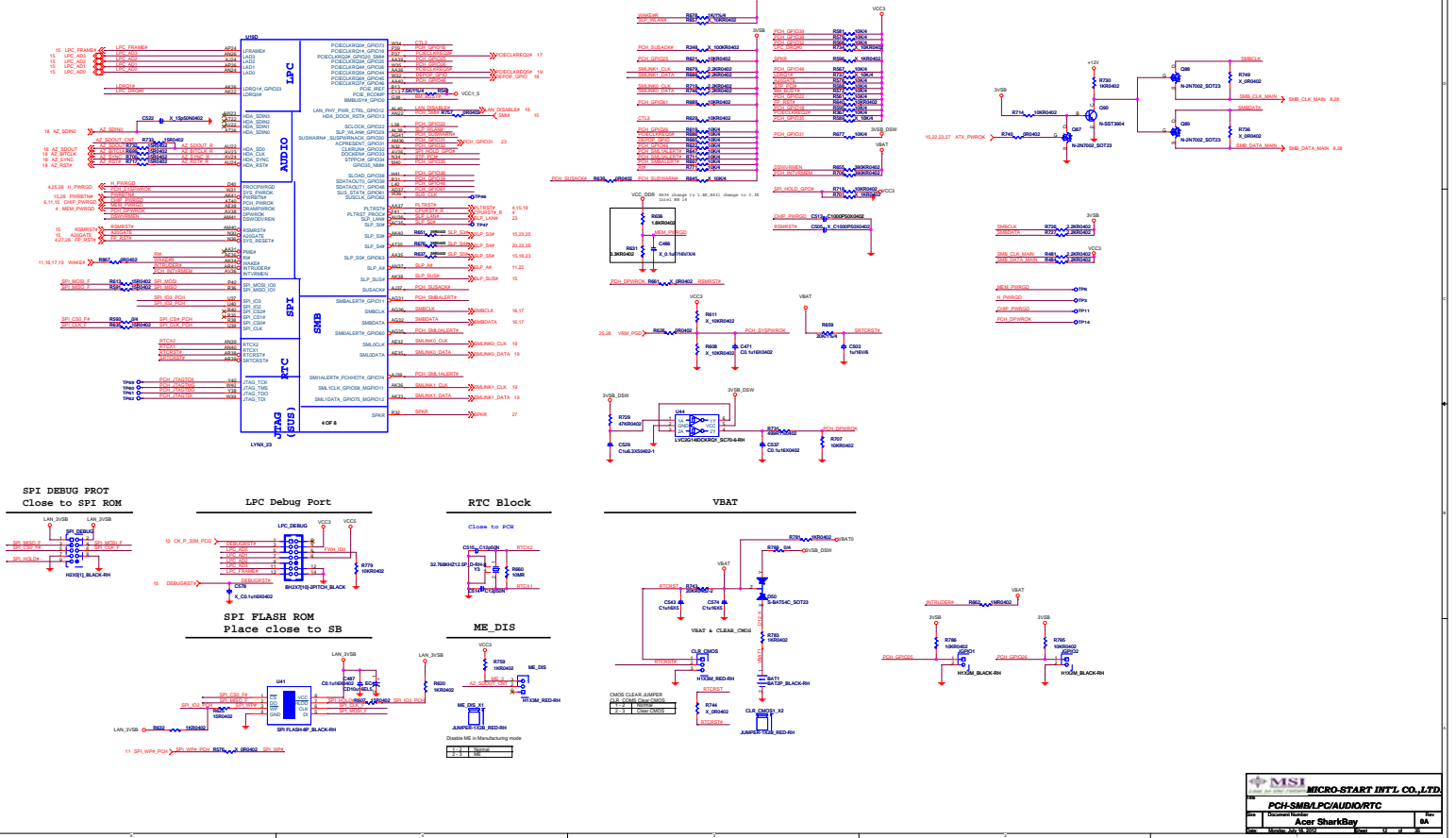
**BIOS STARAPPS**

BIOS STARAPPS	GPI01	GPI06
0A	1	1
NA	0	0

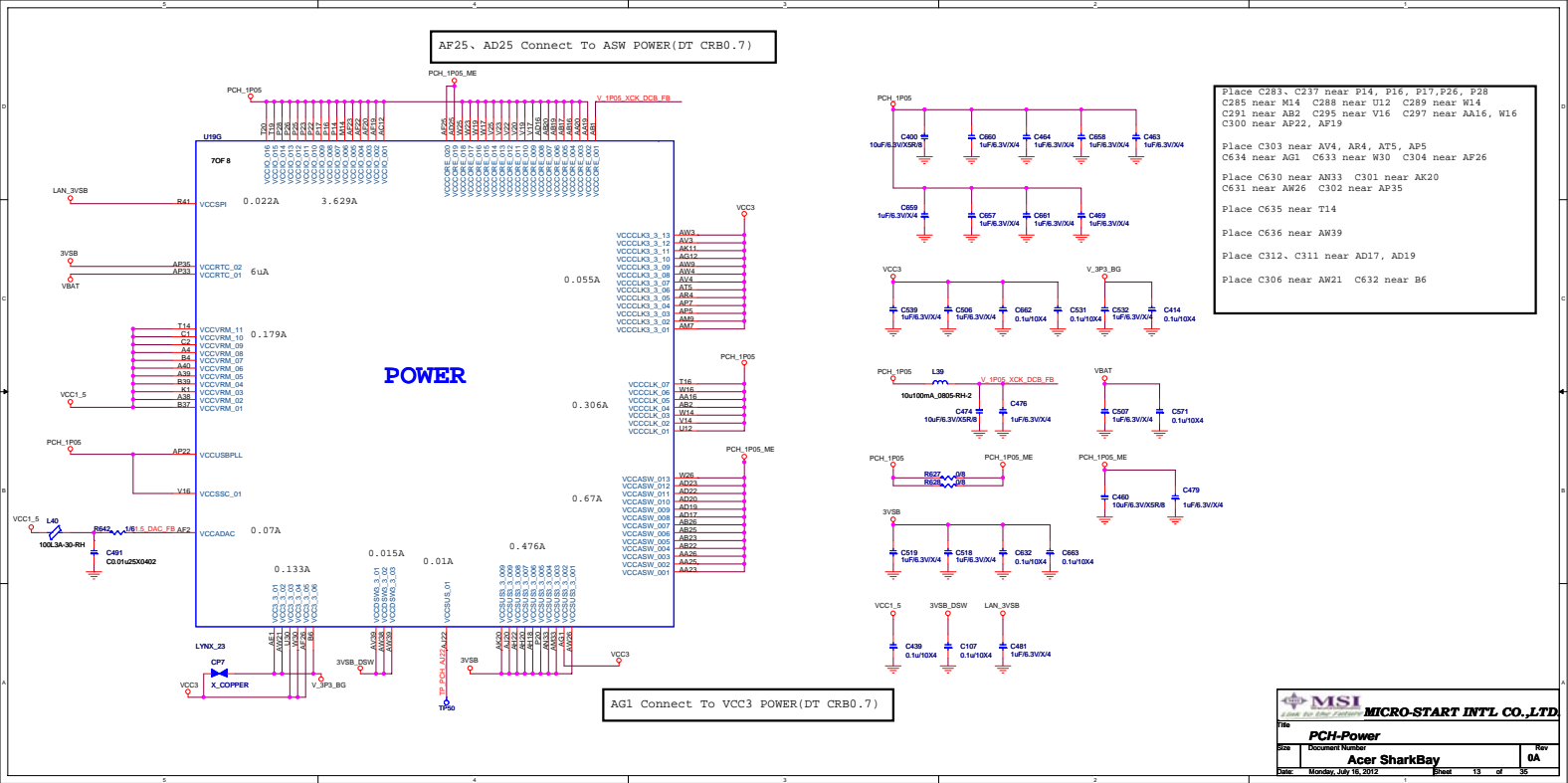
**BIOS Device Select**

BIOS Device	GPI05	GPI09
LPC	1	0
SPI	1	1

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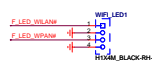
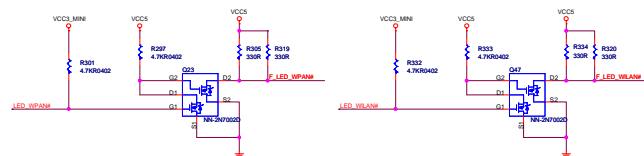
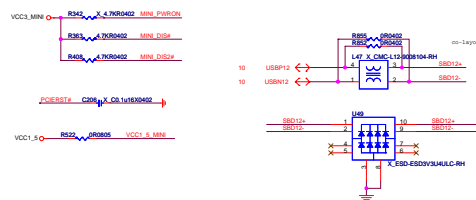
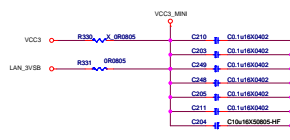
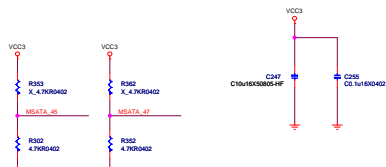
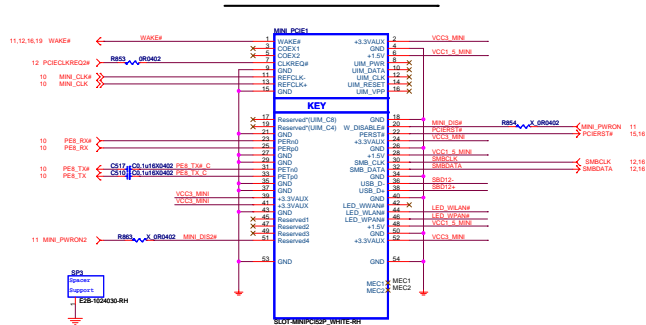
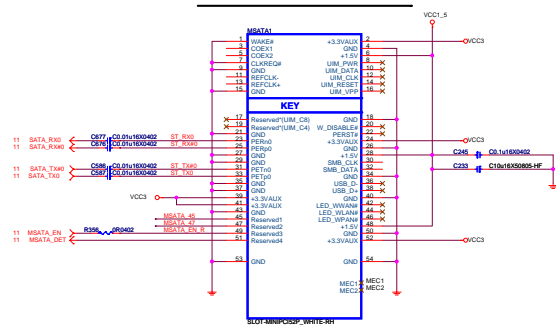
www.aitech1.ru



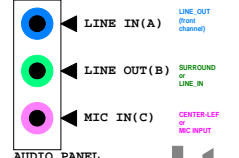
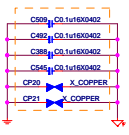
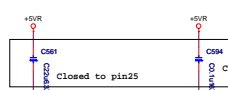
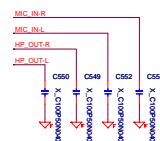
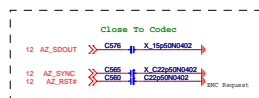
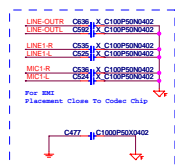
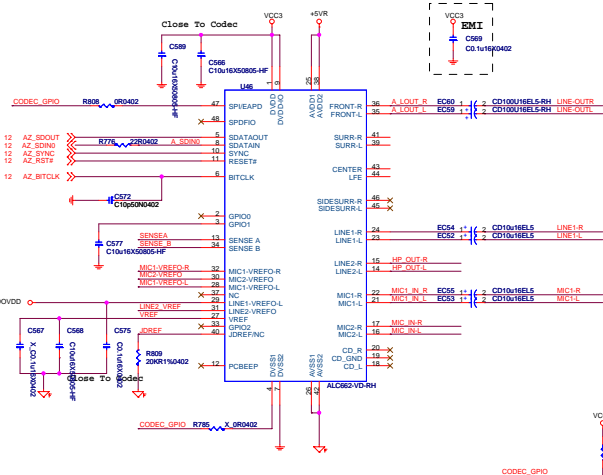
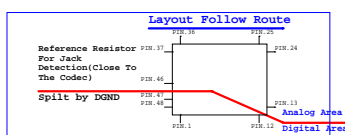


[illegible]

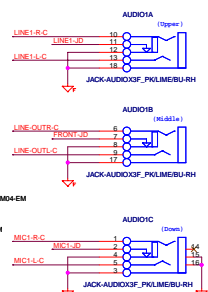
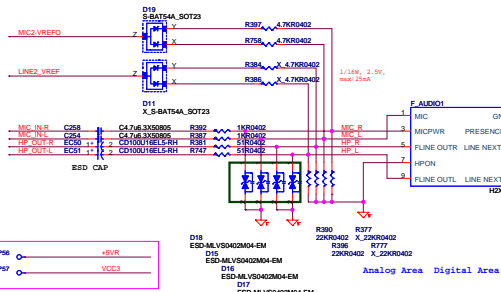




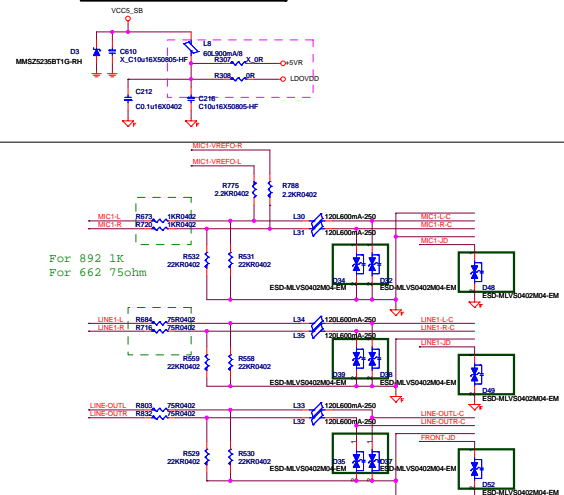
## Azalia Codec -ALC662



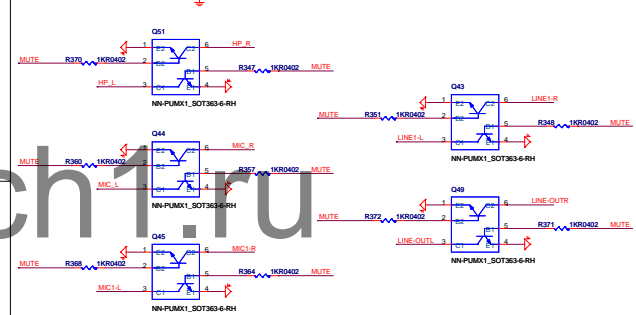
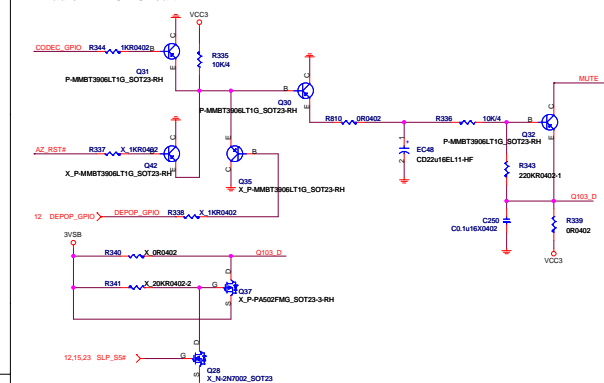
### Front Audio Jack



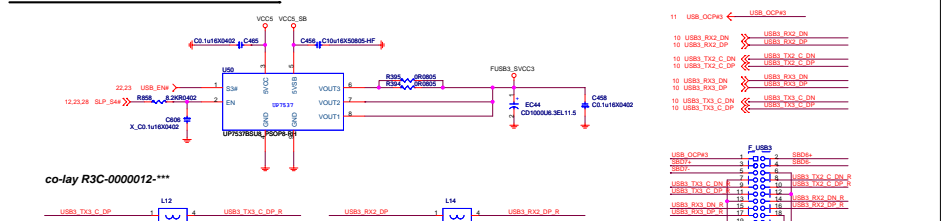
### **AUDIO CODE REGULATORS**



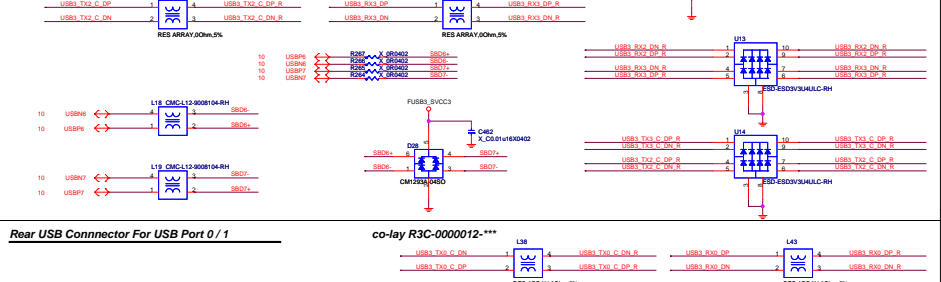
### Audio DE-POP Circuit



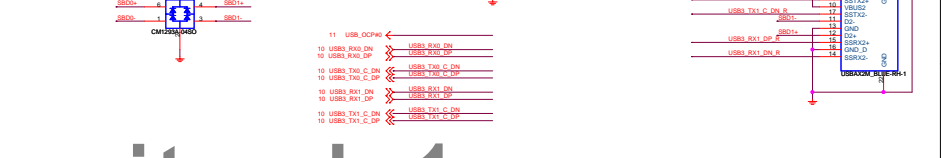
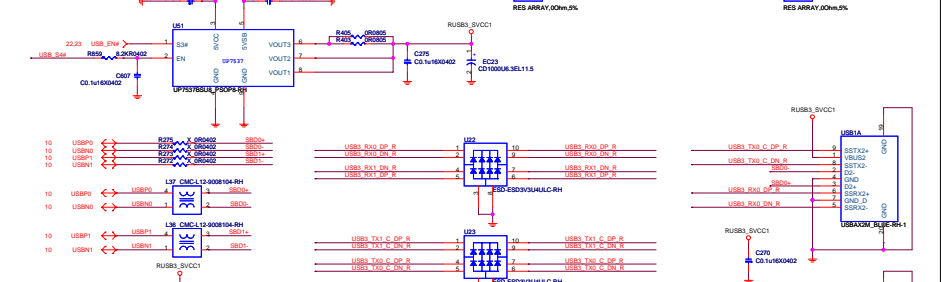




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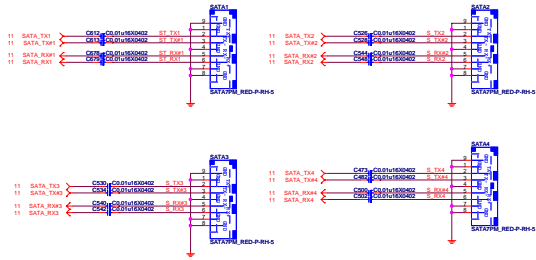
## Rear USB Connector For USB Port 0 / 1



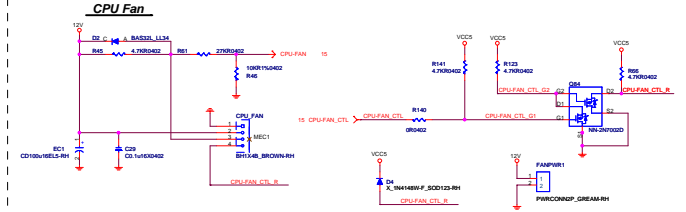
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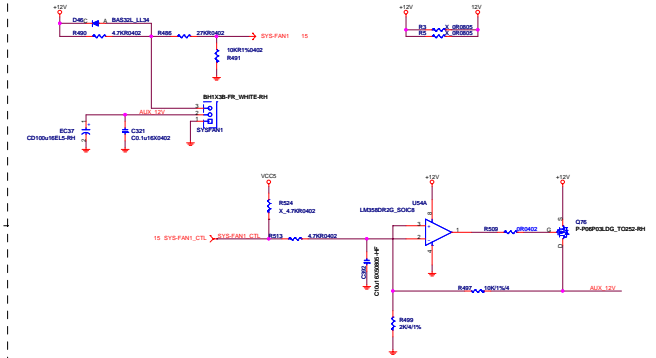
# SATA Connector

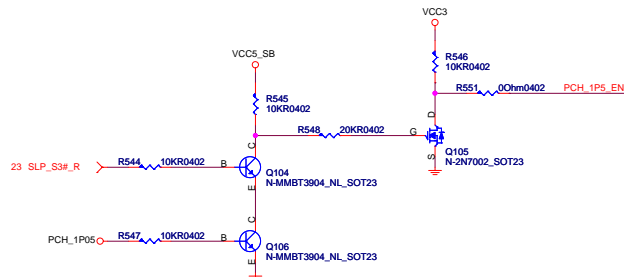


# CPU Fan

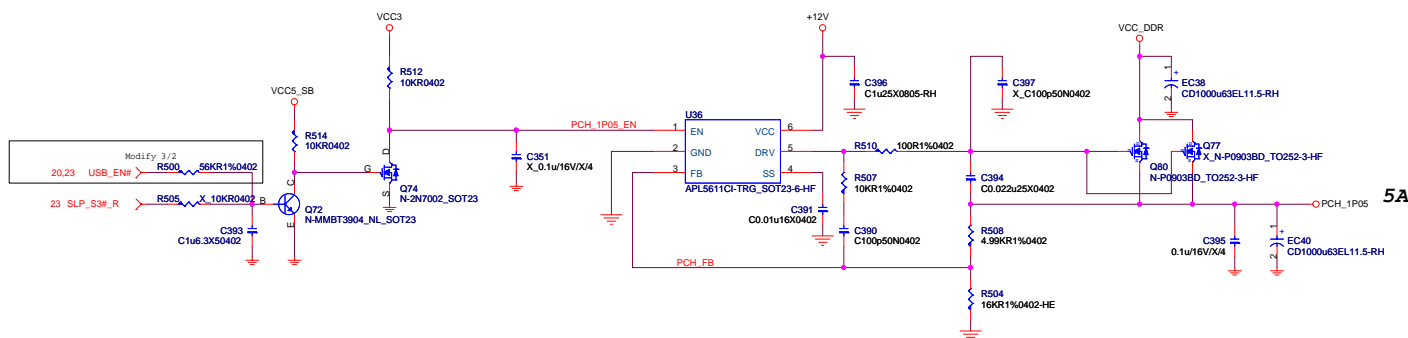


# System Fan





### PCH Core Power



Let ISL8014 go skip mode when power off.

BOTTOM PAD CONNECT TO GND Through 4 VIAS





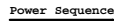
DCM programming pin:

- Ground this pin to setup automatic CCM-DCM transfer without minimum switching frequency limitation;
- Connect this pin to VCC to force CCM operation;
- Leave this pin open to give automatic CCM-DCM transfer, but with minimum switching frequency of 33KHz.





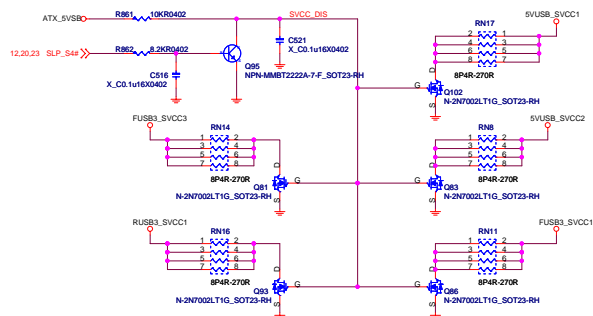
## SharkBay VR12.5 Power Circuit - 4 Phase




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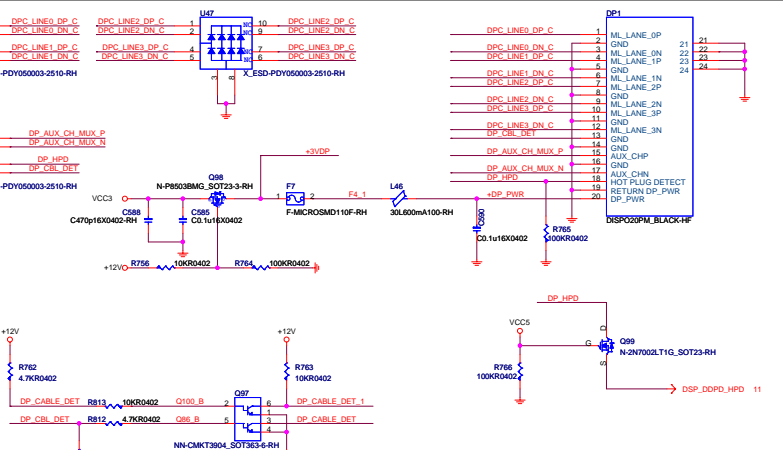
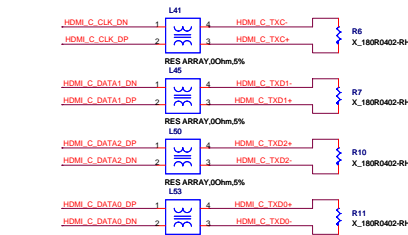
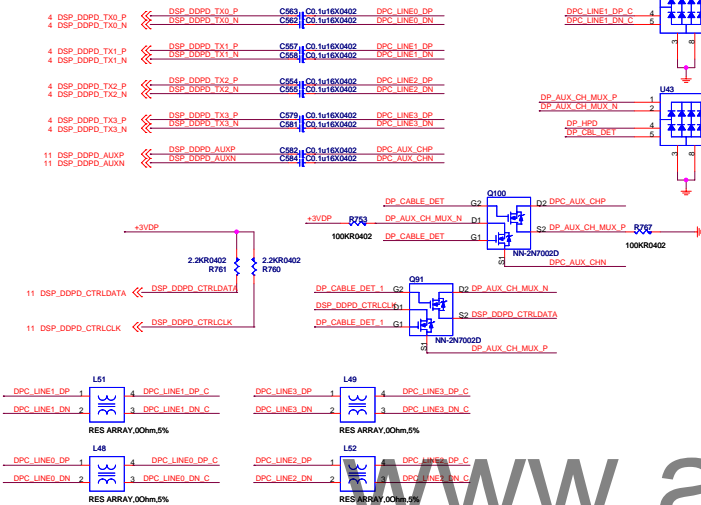


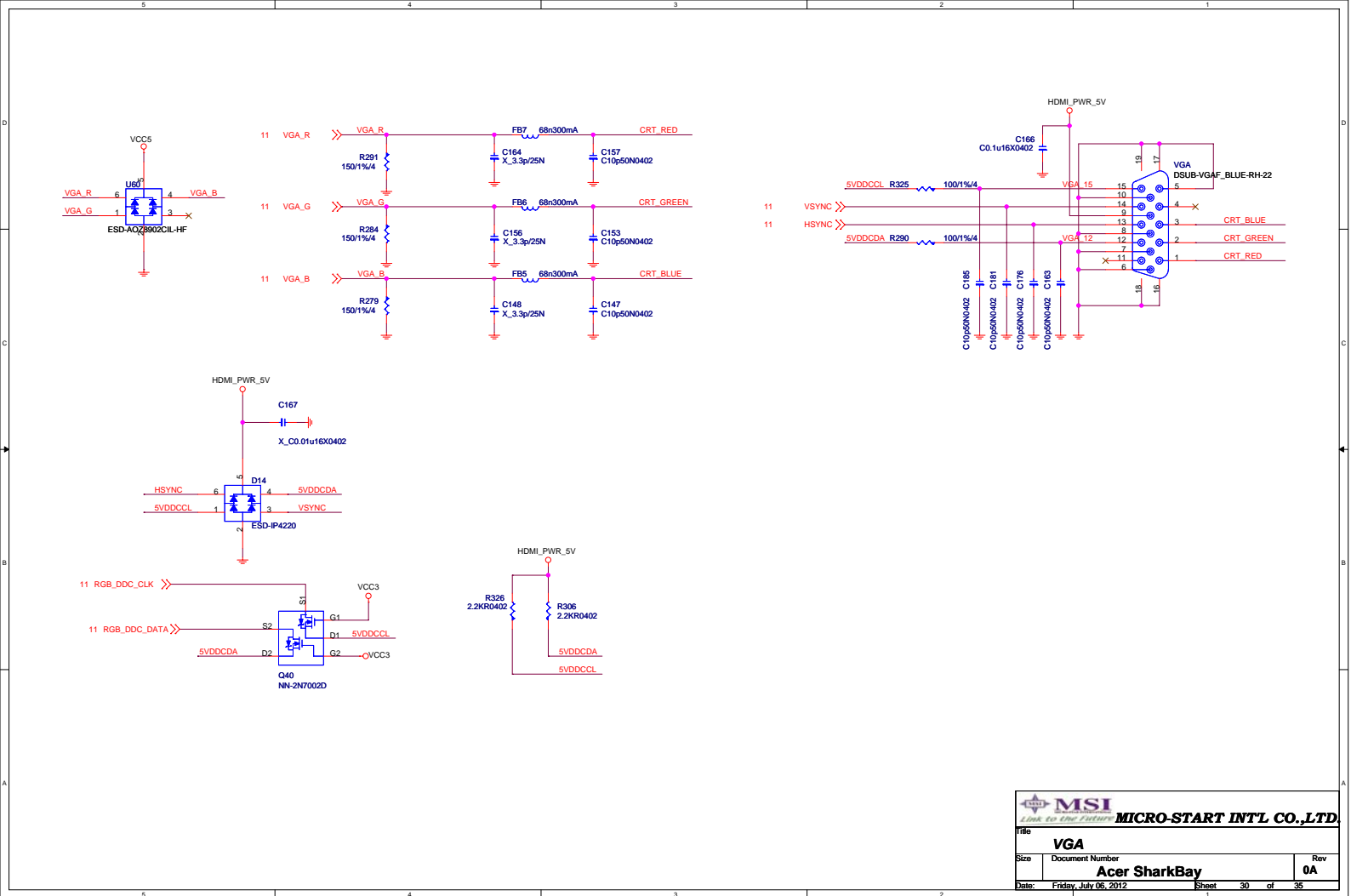




 <b>MICRO-START INT'L CO.,LTD.</b>			
<b>Title</b> <b>CPU/PCH XDP&amp;USB PW-Discharge</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
<b>Acer SharkBay</b>		<b>0A</b>	
<b>Date:</b> Friday, July 08, 2012	<b>Sheet</b> 28	<b>of</b> 35	

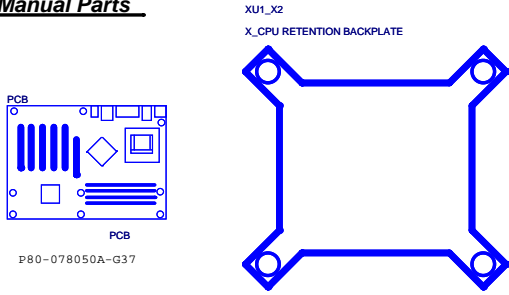
4	HDMI_DDP_C_CLK_P	HDMI DDP_C CLK_P
4	HDMI_DDP_C_CLK_N	HDMI DDP_C CLK_N
4	HDMI_DDP_C_TX2_P	HDMI DDP_C TX2_P
4	HDMI_DDP_C_TX2_N	HDMI DDP_C TX2_N
4	HDMI_DDP_C_TX1_P	HDMI DDP_C TX1_P
4	HDMI_DDP_C_TX1_N	HDMI DDP_C TX1_N
4	HDMI_DDP_C_TX0_P	HDMI DDP_C TX0_P
4	HDMI_DDP_C_TX0_N	HDMI DDP_C TX0_N



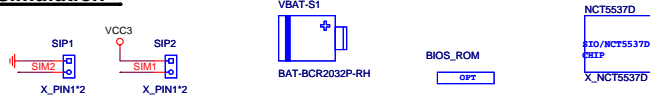


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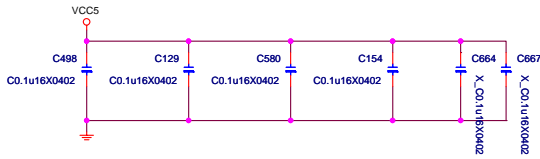
## Manual Parts



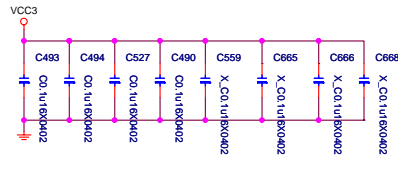
## Simulation



### For EMI

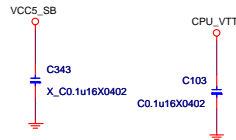


### For Moat CAP

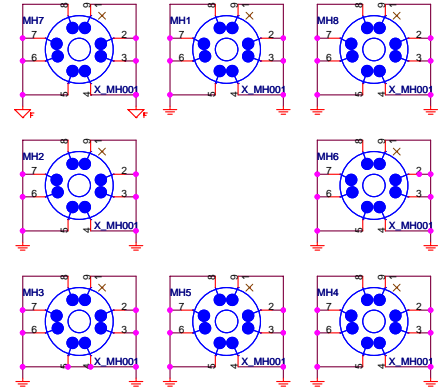


## Optics Orientation Holes

### Optical Fiducial Marks-120



## Mounting Holes



<b>MICRO-START INTL CO.,LTD</b>		
<b>Manual &amp; Option Parts</b>		
Size	Document Number	Rev
	<b>Acer SharkBay</b>	<b>0A</b>
Date:	Monday, July 16, 2012	Sheet 31 of 35

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The timing diagram illustrates the SPI interface signals: CSN (Chip Select Not), SCLK (Serial Clock), and SPI data. The signals are shown for both the Board and the Slave. The diagram includes a note: "NOT USED IN THIS CONFIGURATION".

[illegible][illegible]

```

graph TD
    Processor[Intel 1150 Processor] -- CPU --> PCH[PCH]
    PCH -- SMBus --> SuperIO[Super I/O NCT5533D]
    PCH -- I2C --> ALC[ALC892 HD Codec]
    PCH -- I2C --> Reset[RESET SW]
    PCH -- PCI/PCIe --> CPUDXP[CPU XDP]
    PCH -- PCI/PCIe --> PCHXDP[PCH XDP]
    PCH -- USB --> LAN[LAN 8111P]
    PCH -- USB --> TPM[TPM]
    PCH -- SATA --> AssetID[Asset ID]
    SuperIO -- SATA --> PCHX16[PCH X16 Slot]
    SuperIO -- PCI/PCIe --> PCHX1[PCH X1 Slot]
    SuperIO -- SATA --> MPCI[MPCI/USBATA Slot]
  
```

Timing diagram showing the relationship between various signals and RSMRST#:

- 3VSB\_DSW
- PCH\_DPWROK
- SLP\_SUS#
- /SYS5VSB\_OFF
- 5VSB
- 3VSB
- RSMRST#

Diagram showing the pin connections for the ADXL345 module. The pins are labeled as follows:

- 12V
- 5V
- 3.3V
- 5VDRV1
- VCC1\_5REF
- DDR\_EN
- VCC1\_5
- VCC\_DDR
- PCH\_1P05
- CHIP\_PWRGD
- MEM\_PWRGD
- H\_PWRGD
- VCCCP
- PCH\_SYSPWROK
- SUS\_STAT#
- PLTRST#



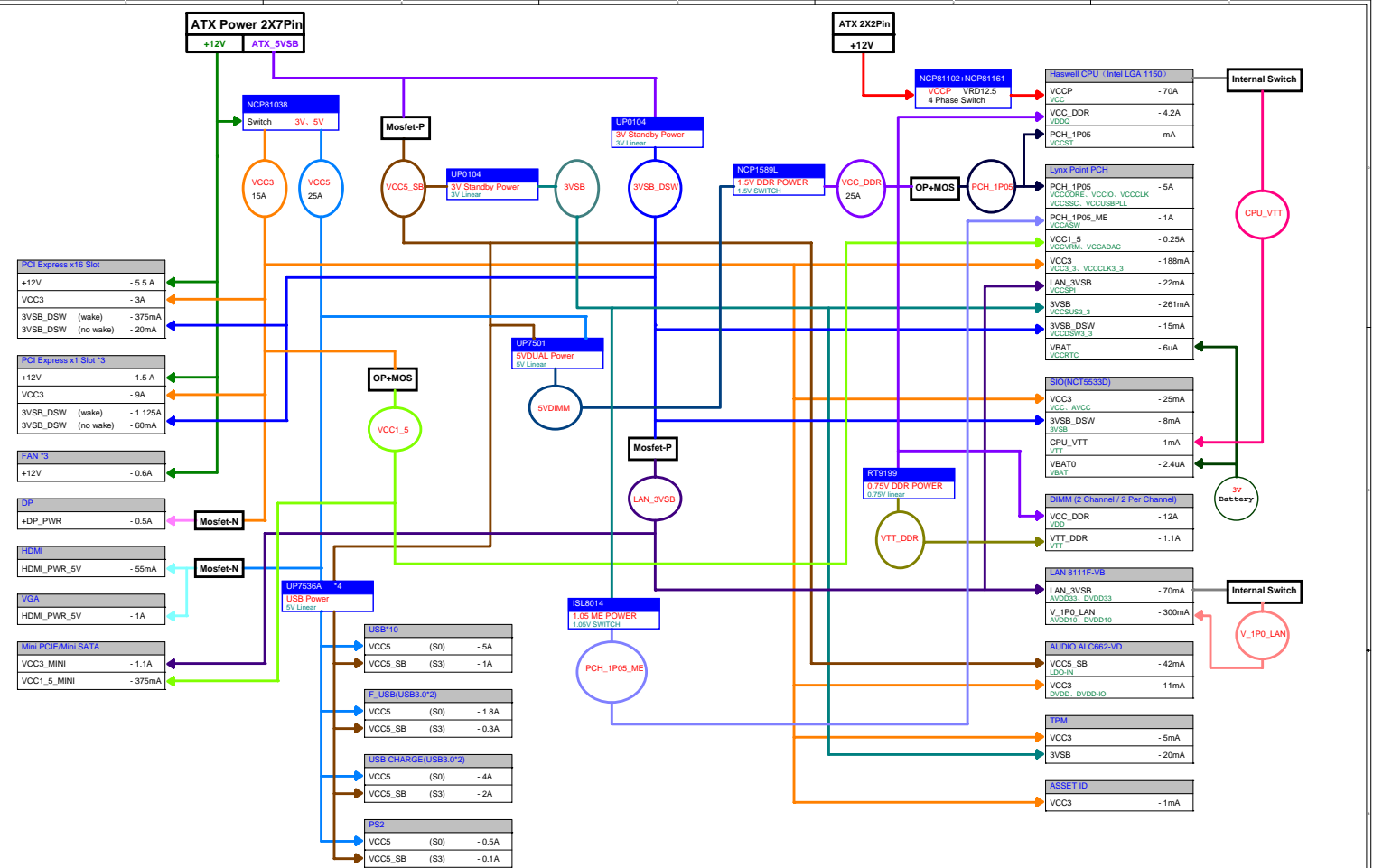
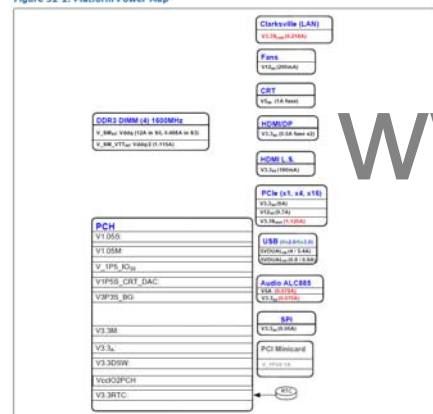



Figure 32-2: Platform Power Map



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<b>History</b>		
File	Document Number	Rev
	<b>Acer SharkBay</b>	<b>0A</b>
Date	Folder, July 06, 2012	Sheet 35 of 35

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